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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,286	02/26/2002	Atsushi Takane	H6808.0004/P004	5346

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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER
JOHNSTON, PHILLIP A

ART UNIT	PAPER NUMBER
2881	

DATE MAILED: 09/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/082,286	TAKANE ET AL.	
	Examiner	Art Unit	
	Phillip A Johnston	2881	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

D tail d Acti n

Specification

1. The disclosure is objected to because of the following informalities: Page 19 line 26, "that the both" should be "that both"; and page 27 line 4,"efficient" should be "coefficient".

Appropriate correction is required.

Drawings

2. The drawings are objected to because of the following minor informalities:

Figures 2 and 4., Ref # 205,405 and 510 is labeled "deteced", and should be "detected". Figure 4. Ref # 409 is labeled "Re-resister template" and should be " Re-register template". Figure 5 Ref # 510 is labeled "Re-resister template" and should be " Re-register template". Figure 17 Ref # 1702 is labeled "desplayed" and should be "displayed". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. Figure 1. and Figure 7. should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claims R jection – 35 U.S.C. 102(b)

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 5, 6, 9, 10, and 19-23 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by U.S. Patent No. 6,154,714 to Lepejian.

Lepejian clearly discloses a semiconductor wafer navigation system that includes all the limitations recited in Claims 1-3, 5, 6, 9, 10, and 19-23. Regarding Claims 1-3, the defect processing system 10 has in-line defect inspection stations 12, 14, 16, and 18, test station 20, and data processing system 22. The defect inspection stations may contain either optical and /or scanning electron microscopes. Once a wafer is examined, data corresponding to any detected defects is either stored by the individual inspection station 12, 14, 16, or 18 which detected the defect, or transmitted to processing system 22 for storage in database 26. Database 26 may contain one large file, or many smaller files segregated by wafer number, layer number, category, type, or any other convenient criteria depending on the needs of the particular manufacturing environment. Lepejian further shows it is most efficient to regularly transmit the data from each inspection station to a central processing location such as database 26, and that it is also possible to hold a predetermined amount of data at each inspection station 12, 14, 16, and 18, the central processor interrogating each station as required to download data when necessary to perform a defect analysis. See Column 3 line 60, and Column 4

lines 20-59. It is well known in the art that the display screen of Claim 3 would be part of the processing system 22 used in the download process.

Regarding Claims 5, 6, 9, 10, 19 and 20. Lepejian clearly shows that data transmitted from database 26 in the central processor at inspection stations 12, 14, 16, and 18 will also contain for any given die, a list of attributes for each noted defect, including the defect's location, size, and layer of detection. In addition to using current and historical defect data, the navigation system uses a wafer definition file 30 which contains GDSII and other information regarding the definition of functional blocks, the size and placement of functional blocks within a die, and the size, orientation, and placement of dice on the wafer, etc. It is well known in the art that GDSII is a standard CAD layout format. In addition, database 26 contains a defect attributes file 32 which is a knowledge base containing the results of experience with manufacturing using a particular integrated circuit process. Information gathered during failure analysis of defects detected at inspection stations 12, 14, 16, and 18 is used to compile a historical knowledge base that contains information relating to all identified defects. Although these files are shown residing on data processing system 22, Lepejian teaches that this file and other files used in the method of the invention may reside on any media in any location, such as on an engineering desktop computer, or networked computer.

Regarding Claims 21-23, Lepejian clearly shows the modification and editing functions of the semiconductor inspection system, performed by in-line inspection stations 12,14, 16, and 18, to determine whether a defect causes fatal or, false fault indications. Each

wafer is loaded into the station at process step 92. Wafer identification data is then read at step 92 by the tester off of the wafer. At step 96, previous inspection data for the wafer is loaded into active memory. In this manner, the wafer definition file 30 is "viewed" at different stages of the manufacturing process allowing the defects detected at a particular process step to be analyzed relative to the design at that particular point in the process. For example, defects detected at the inspection point which follows the deposition of one conductive metal layer are placed within a layout file that contains all layers deposited prior to and including that layer. Each defect is "added" to the layout as a polygon with its positional and knowledge based derived attributes to determine if its introduction effects the net list. When comparisons are made between historical defects and the defect being analyzed, weights are assigned to each of the historical defects, depending upon the relative similarities between any given defects. When a defect is identified as possibly affecting a particular geometry on the circuit, the net list of that particular geometry is extracted from the wafer definition file 30 for one time use during the time that a particular defect is being analyzed. In addition, the system uses an algorithm that eliminates defects that connect portions of the same conducting trace which would falsely identify those defects as fatal defects. See Column 7, lines 11-67 and Column 8, lines 2-56.

Claims Rej ction – 35 U.S.C. 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4, 7, 8, 11, and 12-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No.6,154,714 to Lepejian in view of Okubo, U.S. Patent No. 5,872,862.

Regarding Claims 4, 7, 8, and 11, Lepejian discloses a semiconductor inspection system that includes all the limitations of Claims 4, 7, 8, and 11, but does not teach the use of wafer pattern matching via bitmaps generated from a Scanning Electron Microscope (SEM). Okubo describes a pattern matching apparatus that scans a sample with a Scanning Electron Microscope (SEM) to form a secondary electron image of wiring patterns and matches those patterns with patterns prepared from CAD data. As the electron beam unit 110 scans the sample 112, where secondary electrons emitted from the sample are detected by detector 120, and the output is converted by image input unit 122 into a digital image stored in the SEM image frame memory 123. The digitized SEM image is then displayed on display unit 124. The data stored in SEM memory 123 are read and processed by a computer 125. It is implied that the digital image in SEM image frame memory 123, is the electronic equivalent of a bitmap. CAD data storage 127 stores CAD data that provides photomask wiring patterns.

Computer 125 reads the CAD data out of the CAD data storage 127 according to a specified range, determines magnification Ms of the secondary electron image, sets the magnification Ms in the SEM deflection controller 121, determines a target position of stage 111, sets the target position in the stage controller 126, matches the secondary electron image with the CAD data, and determines a measuring point on the secondary electron image according to a measuring point specified on the CAD data. See column 8 line 1-19. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the wafer navigation system of Lepejian with the wafer pattern matching apparatus of Okubo so that digital images of CAD data could be compared to the secondary electron image from a Scanning Electron Microscope. In so doing, accuracy and repeatability of the inspection system is increased, thereby increasing detect ability of fabrication defects and reliability of predicting the probability that such defects are fatal to the functionality of the die. In addition, inspection time can be reduced through more rapid analysis of circuit connectivity, based on the improved accuracy of determining the location and type of defects relative to a reference CAD layout.

Regarding Claims 12-14, Lepejian in view of Okubo, as applied to claims 4, 7, 8, and 11,discloses a wafer navigation system that includes all the limitations of claims 12-14, but does not teach the use of a pattern matching process with respect to edge images and a smoothing process to make up deformed parts of those images as retrieved from an SEM. Okubo further teaches an edge position detection means 103 that detects edge position Xi of the CAD wiring pattern extending in parallel with an axis Y of a

rectangular coordinate system defined on the CAD data. Secondary electron image storage means 104 stores the secondary electron image of the sample. Projected luminance distribution forming means 105 finds a projected luminance distribution B(X) by accumulating luminance of the secondary electron image along an axis Y of a rectangular coordinate system defined on the secondary electron image. A range of Y may be limited according to secondary electron image magnification accuracy, sample positioning accuracy, and fluctuations in the width of wiring. Edge likelihood detection means 106 detects edge likelihood E(X) of the wiring patterns of the secondary electron image according to the projected luminance distribution B(X). Pattern matching level calculation means 107 computes a pattern matching level V according to the degree of correlation between the edge positions Xi and the edge likelihood E(X). Error detection means 108 changes the edge positions Xi of the CAD wiring patterns depending on the secondary electron image magnification accuracy, sample positioning accuracy, and fluctuations in the width of wiring, to find a maximum pattern matching level V. It is implied here that changing the edge positions Xi of the CAD wiring patterns relative to the secondary electron image position is equivalent to re-registering of the image defined in claim 15. It is also well known in the art that the SEM's secondary electron images can be deformed if there is an error in orthogonality of the X and Y deflection coils of the deflector 317, or if there is a difference in the sensitivity characteristics of the X and Y deflection coils, or if there is an error in parallelism between an axis X of the stage 311 and an axis X of the sample 312 placed on the stage 311. Okubo also teaches a technique for correcting the deformation of the secondary electron image

based on the use of a secondary electron

image corrector, consisting of registers 3214, 3215, 3219, and 321b, which are automatically set by the computer 325 to correct deformation of the secondary electron image through precise control of the beam deflection controller 321. See Column 18, line 56-64. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the wafer navigation system of Lepejian with the wafer pattern matching process of Okubo having edge detection and smoothing processes to correct images retrieved from an SEM. Thereby providing means for obtaining, greater accuracy and repeatability of wafer pattern matching, which is highly desirable in navigation for failure analysis, because the time required for wafer scanning and inspection increases as the size of wafers increases and the number of die on each wafer increases. In addition, as the size of each die shrinks, the number and kind of defects that can affect the operation of the die have also increased. The resulting improved precision in the alignment of the SEM scanned wafer patterns, directly improves the accuracy of locating and identifying defects, which Lepejian recognizes as expected features to be gained from modifying the Lepejian method of wafer navigation with the Okubo pattern matching process.

Regarding claims 15-18, Lepejian in view of Okubo, as applied to claims 12-14 above, discloses a semiconductor inspection system that includes all the limitations of Claims 15-18, but does not teach the reregistering of wafer pattern images to a position of the edge image detected by the matching process between the edge image and the design data. However, Okubo teaches an edge position detection means 103 that is used with

pattern matching level calculation means 107 to compute a pattern matching level V according to the degree of correlation between the edge positions Xi and the edge likelihood E(X). Error detection means 108 then changes the edge positions Xi of the CAD wiring patterns depending on the secondary electron image magnification accuracy, sample positioning accuracy, and fluctuations in the width of wiring, to find a maximum pattern matching level V. This process is then repeated to provide a corrected SEM secondary electron image. For example, wiring patterns 351 and 352 contained in a secondary electron image 350 before correction become wiring patterns 361 and 362 contained in a secondary electron image 360 after the correction. See Column 19, line 62, and Column 20, line 6-11. It is implied here that changing the edge positions Xi of the CAD wiring patterns relative to the secondary electron image position to provide corrected images is equivalent to "re-registering of the image" as defined in claim 15. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the wafer navigation system of Lepejian with the wafer pattern matching process of Okubo, having repeated re-registration of wafer pattern images to a position of the edge image detected by the matching process between the edge image and the design data, to provide corrected images for wafer inspection on a continuous basis. In so doing, wafer capture and inspection can be carried out automatically, quickly and correctly using the Okubo matching process. The importance of the resultant improvement in the semiconductor quality control process is better understood when it is realized that during a typical production cycle, the selected wafers may be scanned as many as 40 times throughout the manufacturing process.

Having rapid and accurate SEM images continuously available to in-process inspectors would allow real-time, on-line fault probability computation and immediate determination as to whether defect limits have been exceeded. Subsequent yield projections would be defined faster and earlier in the process, allowing the decisions to be made earlier and faster, as they relate to continuing or canceling further processing of the wafer, leading ultimately to significant increases in product throughput and reduced quality cost.

Conclusion

8. Any inquiry concerning this communication or earlier communications should be directed to Phillip Johnston whose telephone number is (703) 305-7022. The examiner can normally be reached on Monday-Friday from 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiners supervisor John Lee can be reached at (703) 308-4116. The fax phone numbers are (703) 308-2864 and (703) 308-7721.

JOHN R. LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800